Fig. 1

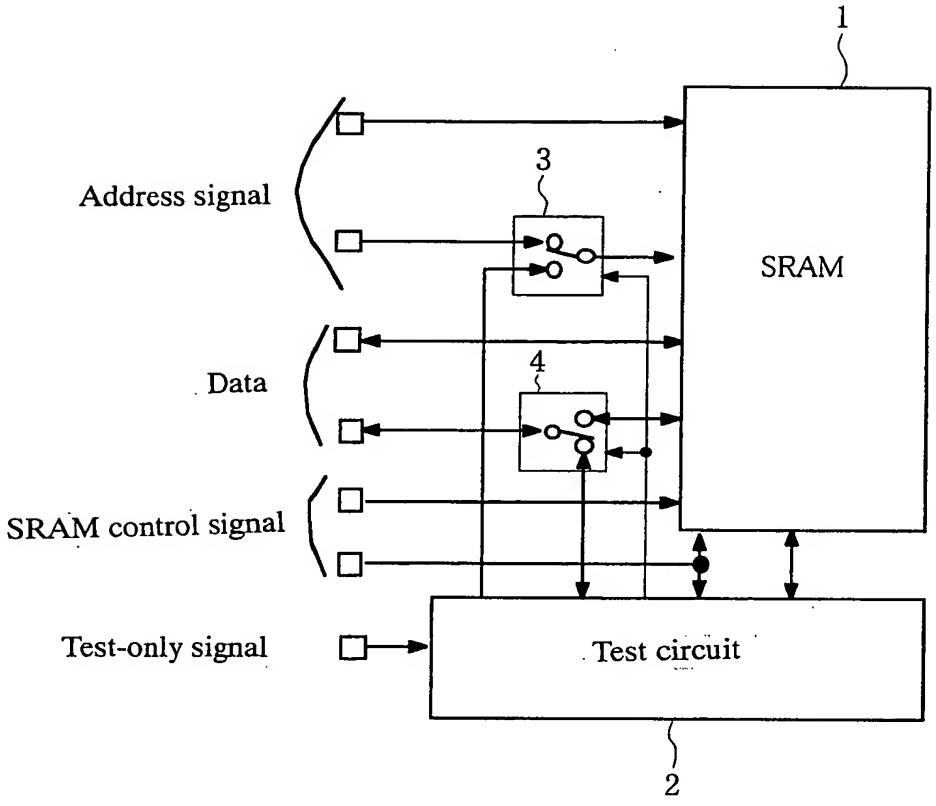

1
Address signal
3
SRAM
Data
4
SRAM control signal
Test-only signal
Test circuit
2

Fig. 2

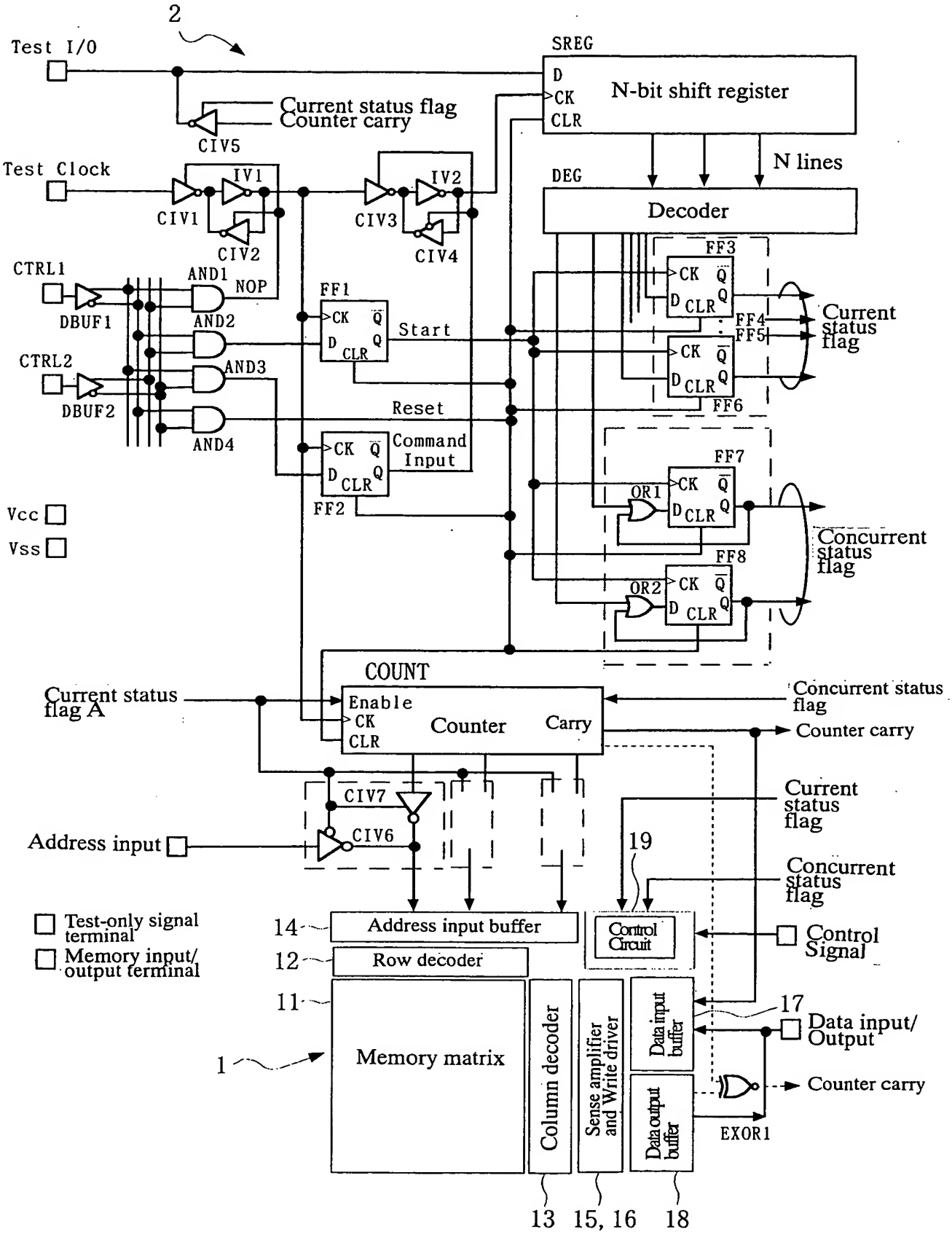

2
Test I/O
SREG
D
CK
CLR
N-bit shift register
Current status flag
Counter carry
CIV5
Test Clock
IV1
IV2
CIV1
CIV2
CIV3
CIV4
N lines
DEG
Decoder
CTRL1
AND1
NOP
DBUF1
AND2
FF1
Start
FF3
FF4
FF5
FF6
Current status flag
CTRL2
AND3
DBUF2
AND4
Reset
Command Input
FF2
FF7
OR1
FF8
OR2
Concurrent status flag
Vcc
Vss
COUNT
Current status flag A
Enable
CK
CLR
Counter
Carry
Concurrent status flag
Counter carry
CIV7
CIV6
Address input
19
Current status flag
Concurrent status flag
Test-only signal terminal
Memory input/ output terminal
14
Address input buffer
Control Circuit
Control Signal
12
Row decoder
11
17
Data input/ Output
1
Memory matrix
Column decoder
Sense amplifier and Write driver
Data input buffer
Data output buffer
Counter carry
EXOR1
13
15, 16
18

Fig. 3

Test Clock	CTRL1	CTRL2	Test I/O	Command register	Status
X	0	0	X	Reset to 000	Reset of test circuit, Deactivation of test circuit
L→H	0	1	X	Set of input command	Operational start of test circuit
L→H	1	0	Command input	Input of TEST I/O	Reception of test command
L→H	1	1	X	No change	NOP

Fig. 4

Test mode	Test command			Status of test circuit	Function of Test I/O at test mode
	1st·Cyc	2nd·Cyc	3rd·Cyc		
Current mode	0	0	0	Deactivation of test circuit	Memory data terminal
	0	0	1	Burn-in (Write) operation	Borrow output of address counter
	0	1	0	Burn-in (Read) operation	Borrow output of address counter
	0	1	1	Monitor burn-in operation	0: PASS 1: Fail output
Concurrent mode	1	0	0	Establishment of multi-choice mode flag	In conformity to current mode
	1	0	1	Establishment of redundant bit mode flag	
	1	1	0	Outside regulation	
	1	1	1	Outside regulation	

Fig. 5

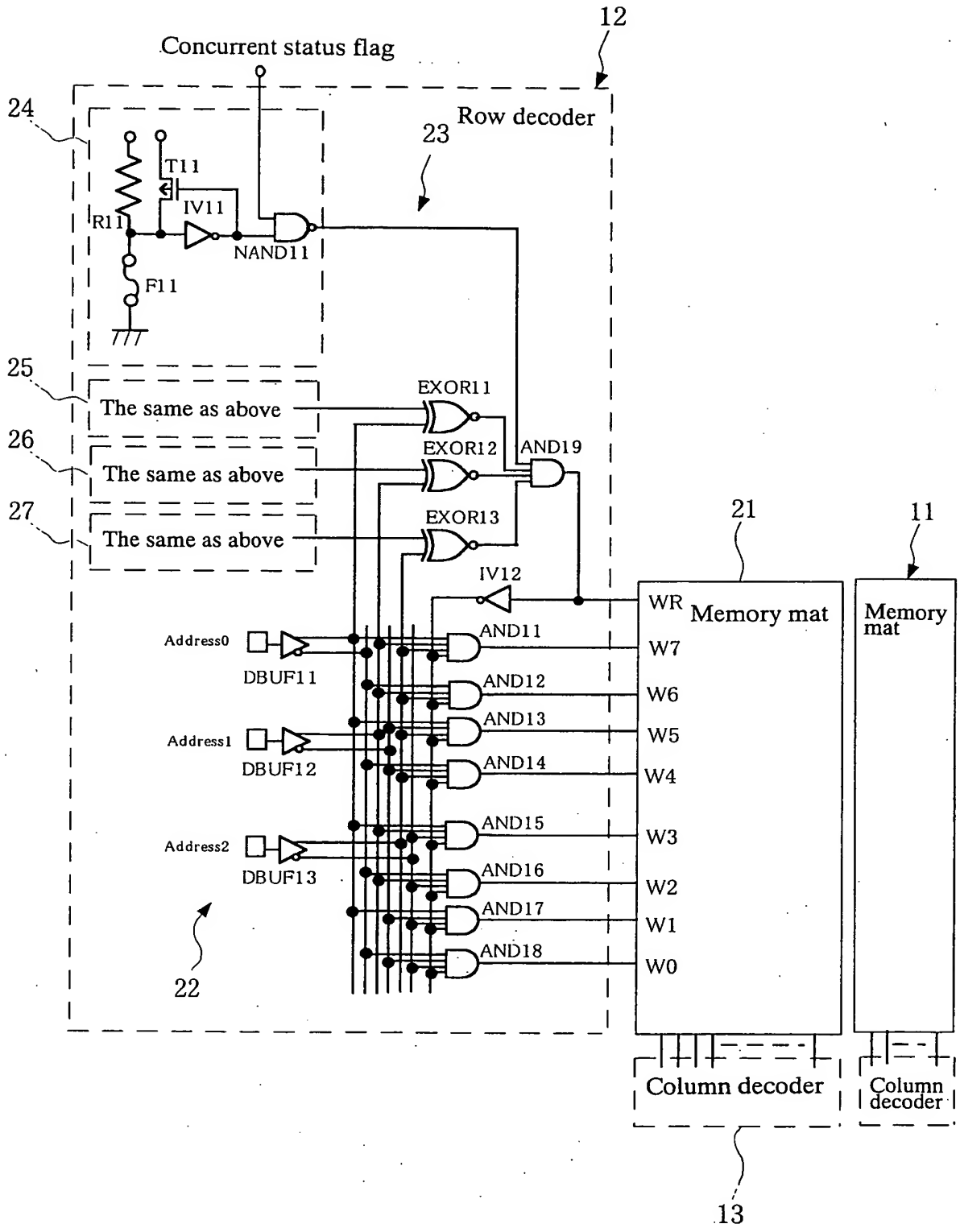

12
Concurrent status flag
24
Row decoder
23
T11
IV11
R11
NAND11
F11
25
The same as above
26
The same as above
27
The same as above
EXOR11
EXOR12
AND19
EXOR13
IV12
21
11
WR
Memory mat
Memory mat
Address0
DBUF11
AND11
W7
AND12
W6
Address1
DBUF12
AND13
W5
AND14
W4
AND15
W3
Address2
DBUF13
AND16
W2
AND17
W1
AND18
W0
22
Column decoder
Column decoder
13

Fig. 6

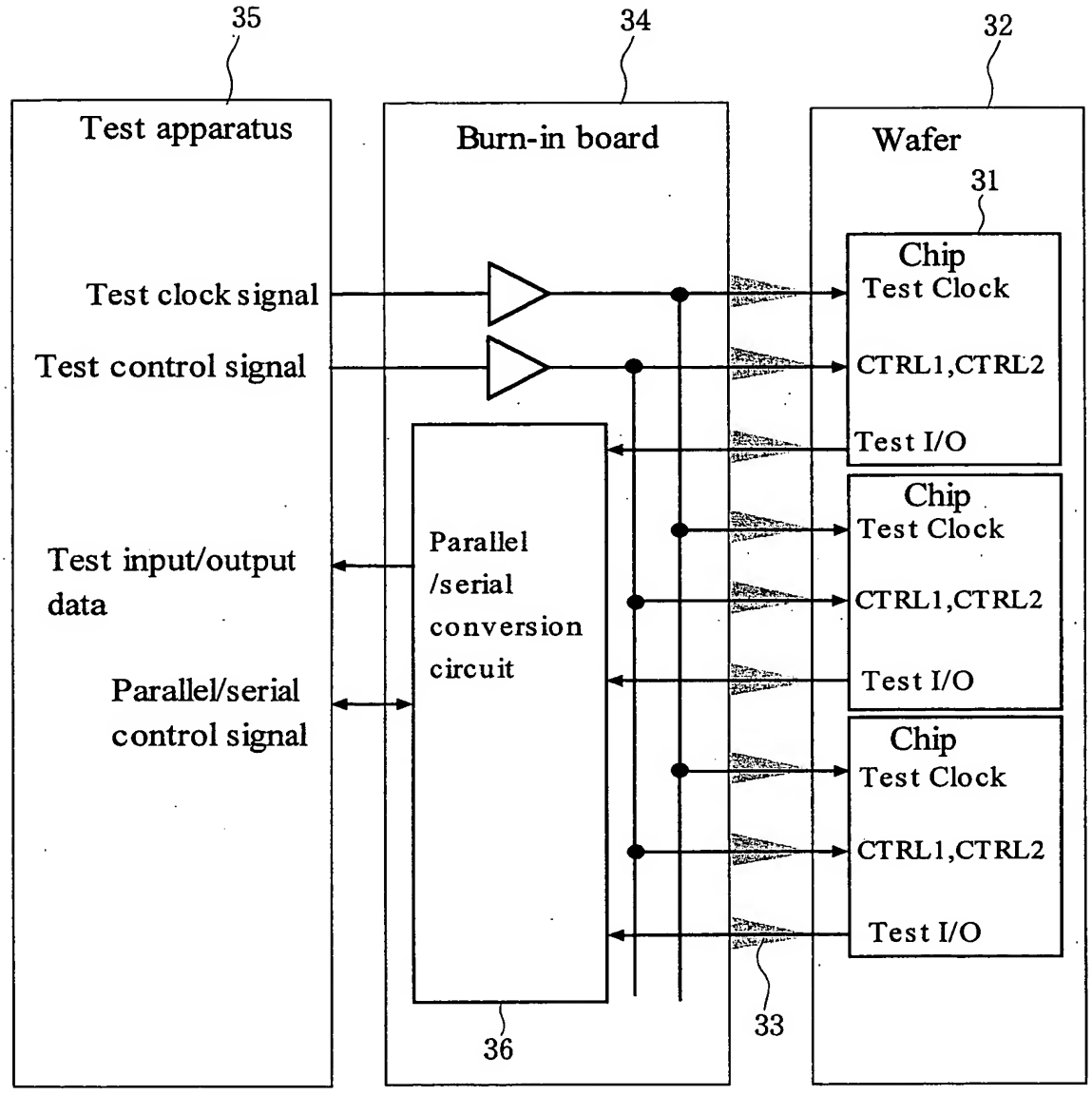

35
34
32
Test apparatus
Burn-in board
Wafer
31
Chip
Test Clock
CTRL1,CTRL2
Test I/O
Test clock signal
Test control signal
Test input/output data
Parallel/serial control signal
Parallel /serial conversion circuit
36
33

Fig. 7

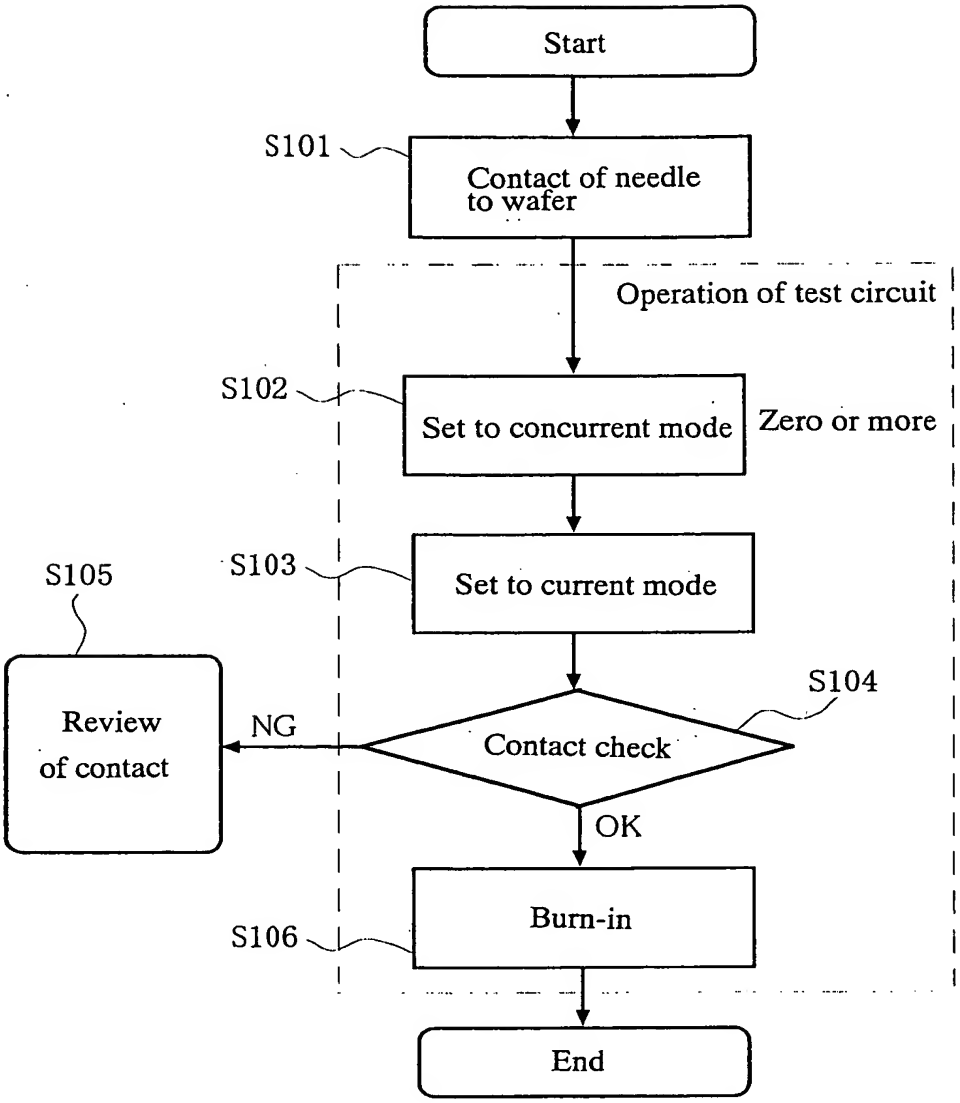

Start
S101
Contact of needle to wafer
Operation of test circuit
S102
Set to concurrent mode
Zero or more
S103
Set to current mode
S105
S104
Review of contact
NG
Contact check
OK
Burn-in
S106
End

Fig. 8

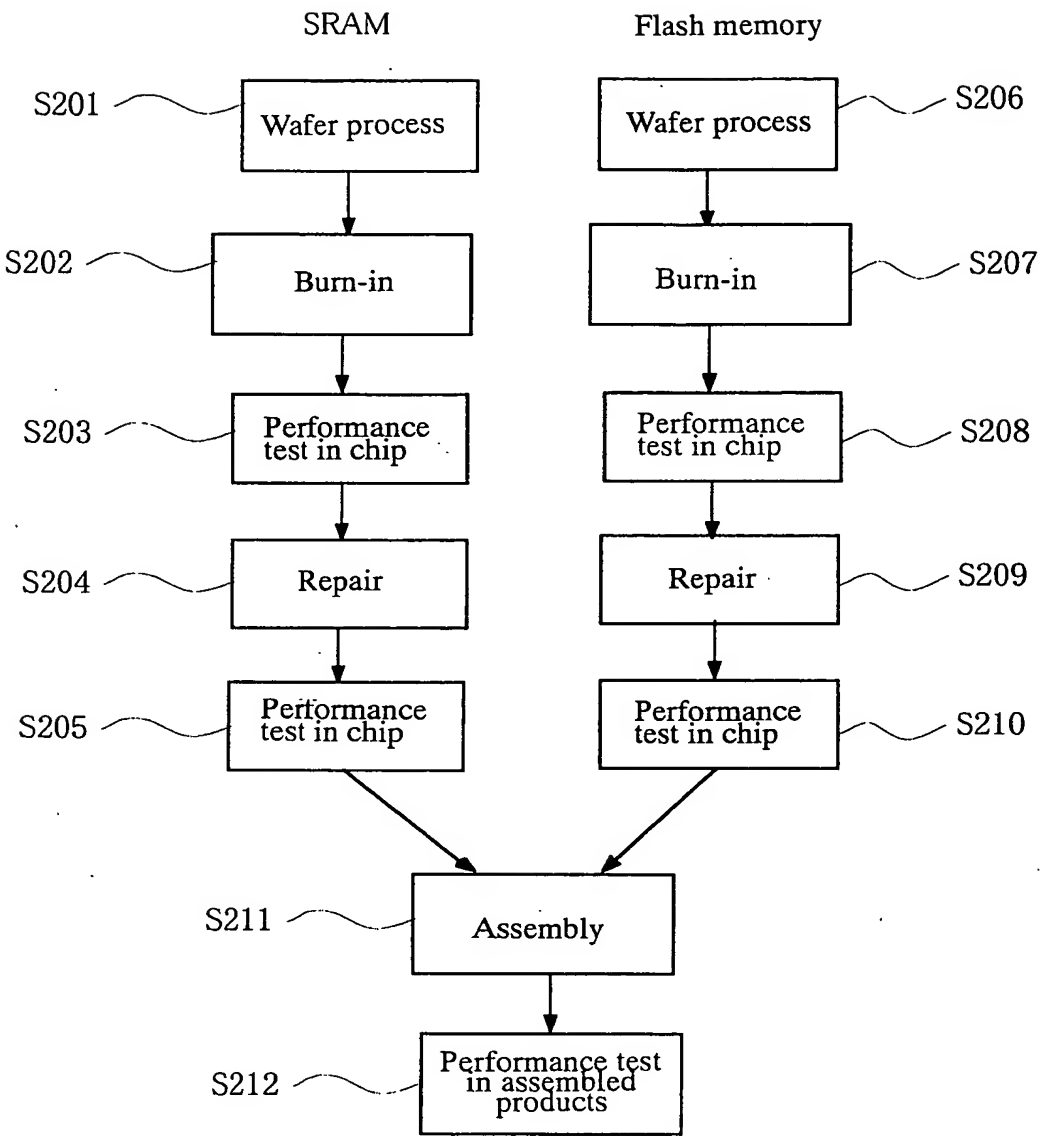

SRAM
Flash memory
S201
Wafer process
S206
Wafer process
S202
Burn-in
S207
Burn-in
S203
Performance test in chip
S208
Performance test in chip
S204
Repair
S209
Repair
S205
Performance test in chip
S210
Performance test in chip
S211
Assembly
S212
Performance test in assembled products

Fig. 9

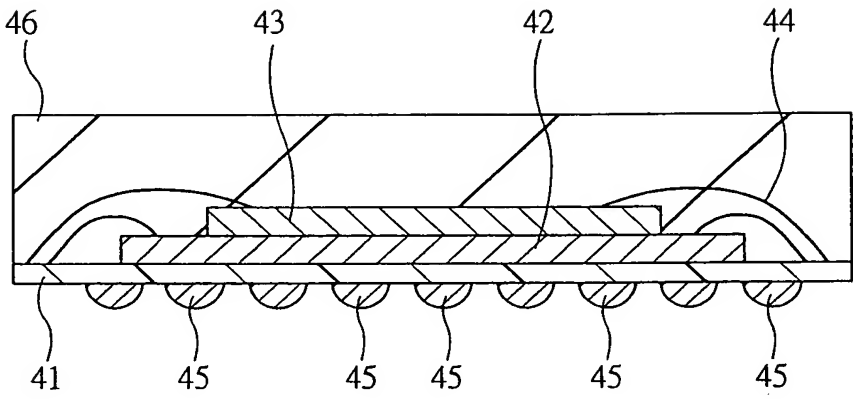


Fig. 10

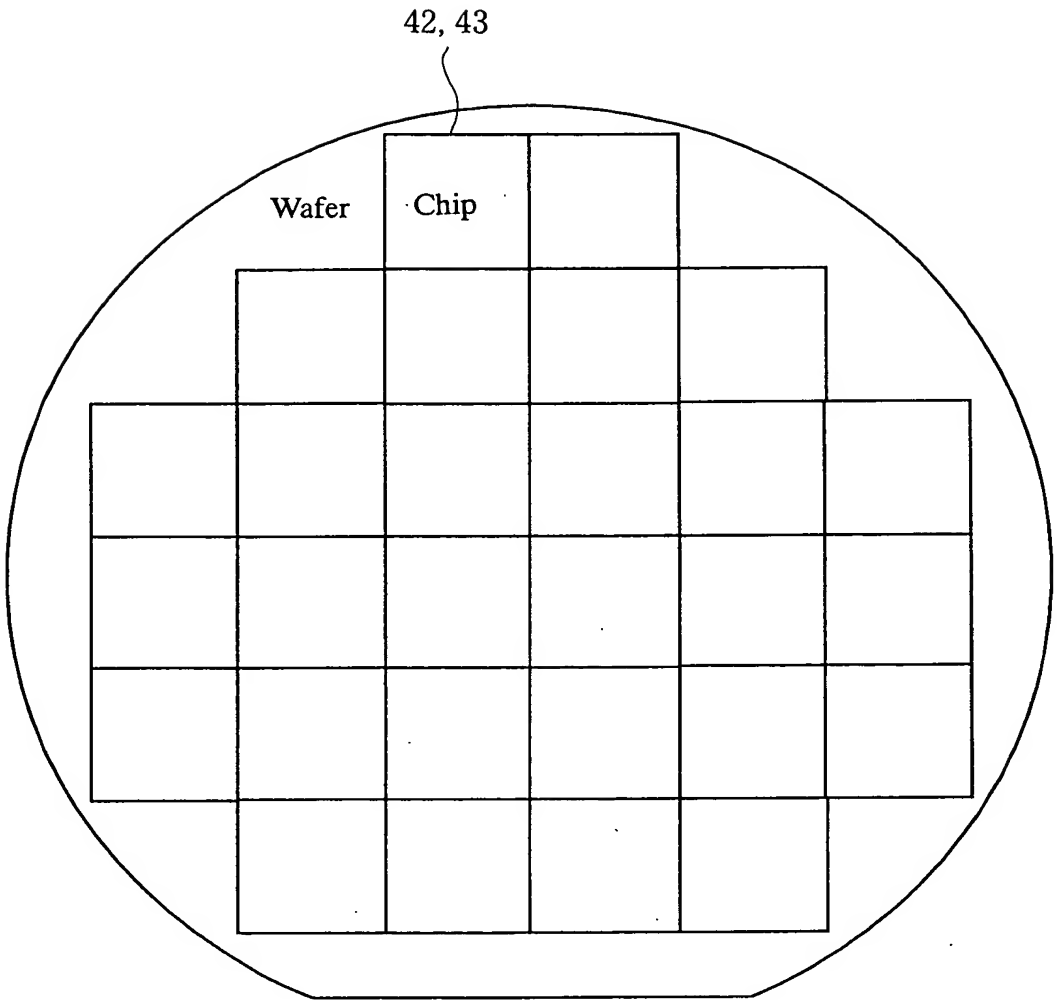


Fig. 11

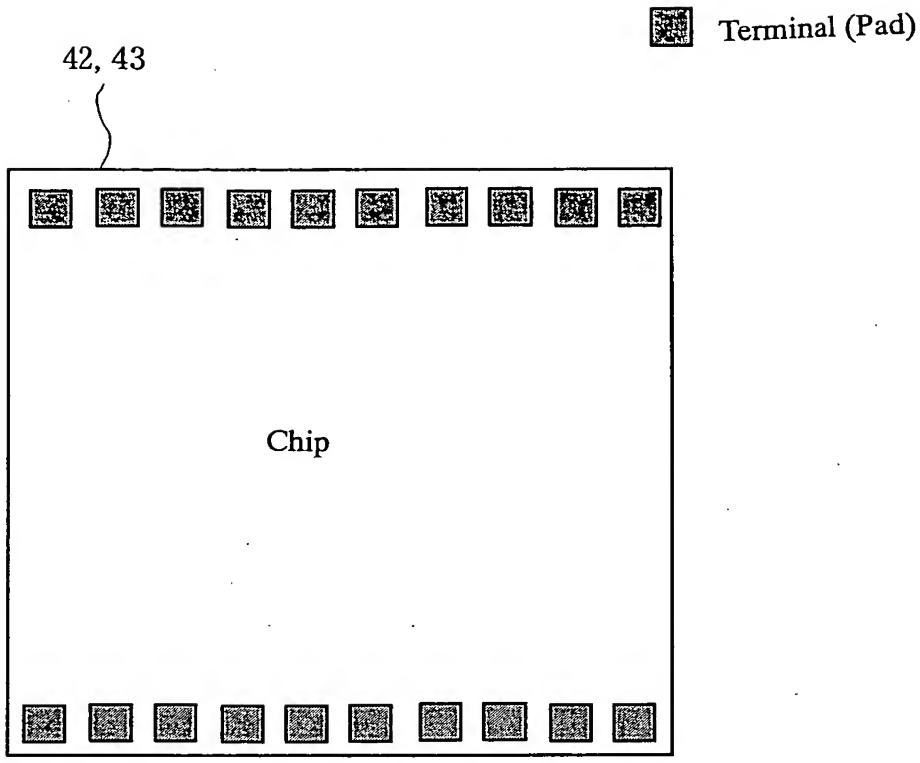


Fig. 12

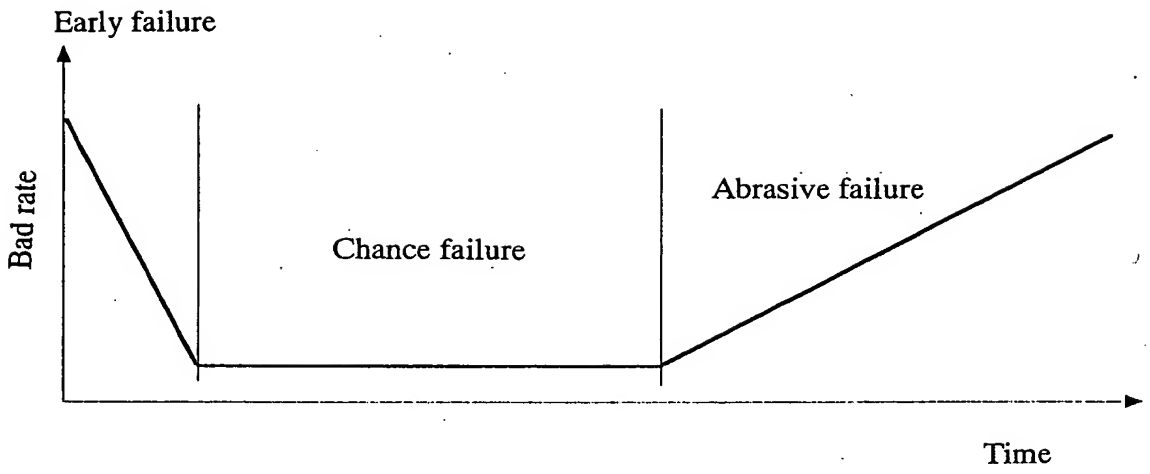

Early failure
Bad rate
Chance failure
Abrasive failure
Time

Fig. 13

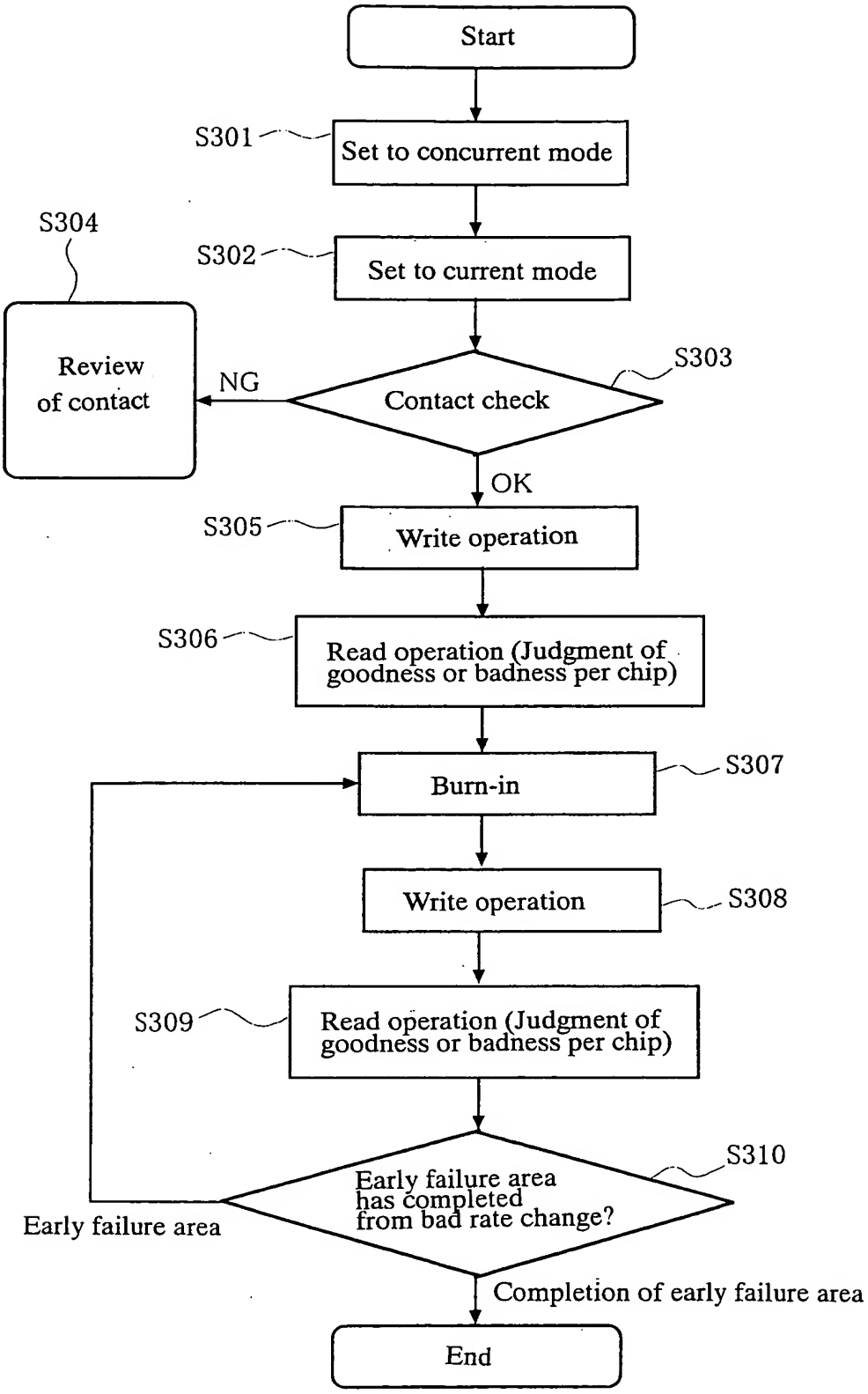

Start
S301
Set to concurrent mode
S304
S302
Set to current mode
Review of contact
NG
Contact check
S303
OK
S305
Write operation
S306
Read operation (Judgment of goodness or badness per chip)
Burn-in
S307
Write operation
S308
S309
Read operation (Judgment of goodness or badness per chip)
S310
Early failure area has completed from bad rate change?
Early failure area
Completion of early failure area
End

Fig. 14

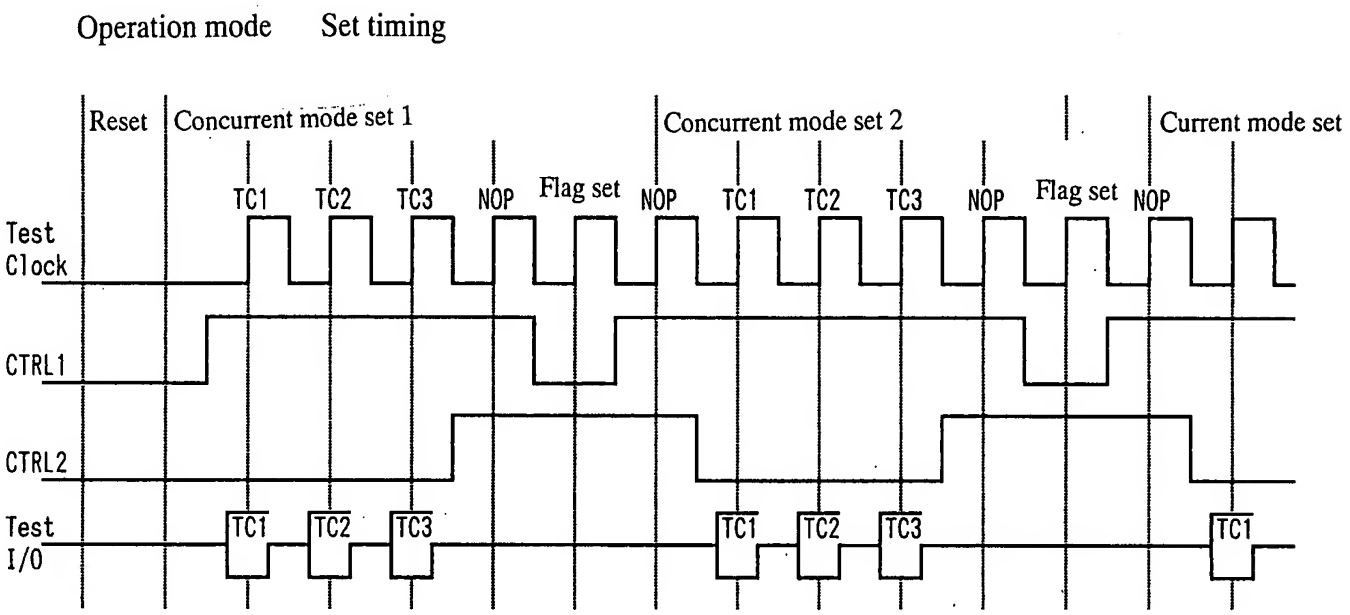

Operation mode
Set timing
Reset
Concurrent mode set 1
Concurrent mode set 2
Current mode set
TC1
TC2
TC3
NOP
Flag set
NOP
TC1
TC2
TC3
NOP
Flag set
NOP
Test Clock
CTRL1
CTRL2
Test I/O
TC1
TC2
TC3
TC1
TC2
TC3
TC1

Fig. 15

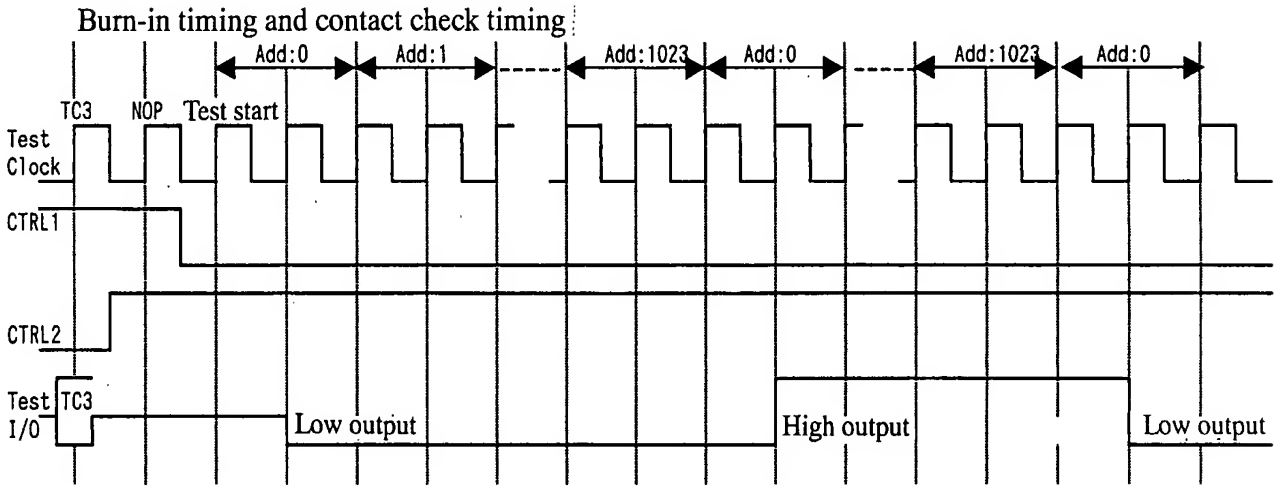

Burn-in timing and contact check timing
Add:0
Add:1
Add:1023
Add:0
Add:1023
Add:0
TC3
NOP
Test start
Test Clock
CTRL1
CTRL2
Test I/O
TC3
Low output
High output
Low output

Fig. 16

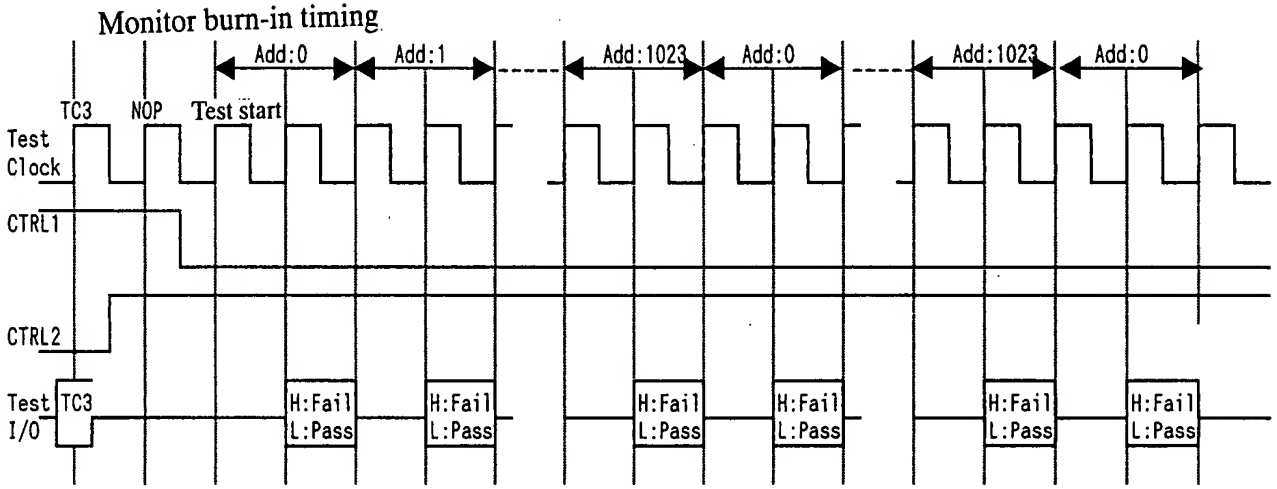

Monitor burn-in timing
Add:0
Add:1
Add:1023
Add:0
Add:1023
Add:0
TC3
NOP
Test start
Test Clock
CTRL1
CTRL2
Test I/O
TC3
H:Fail
L:Pass

Fig. 17

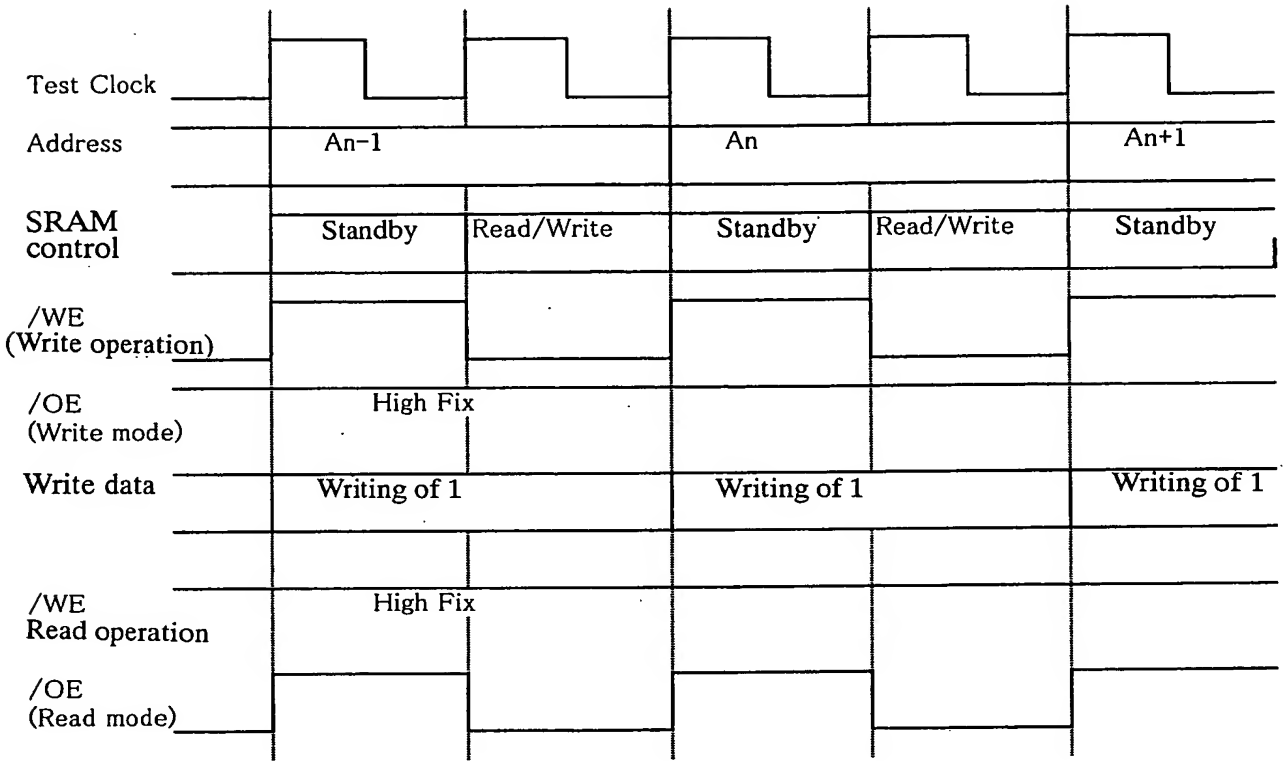

Test Clock
Address
An-1
An
An+1
SRAM control
Standby
Read/Write
Standby
Read/Write
Standby
/WE (Write operation)
/OE (Write mode)
High Fix
Write data
Writing of 1
Writing of 1
Writing of 1
/WE Read operation
High Fix
/OE (Read mode)

Fig. 18

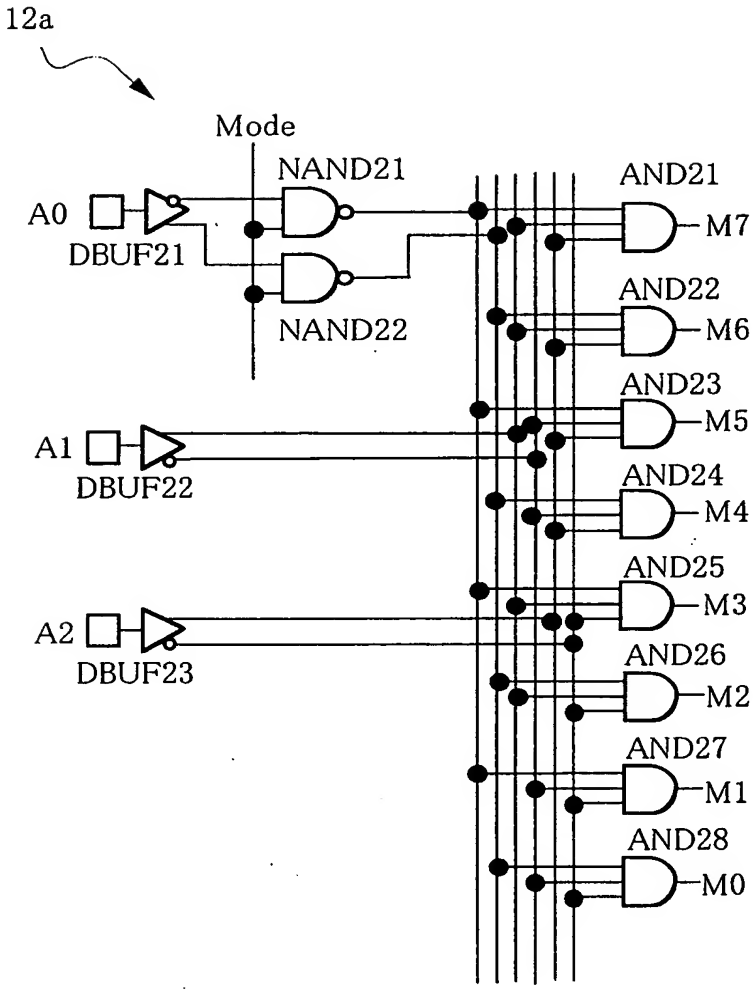
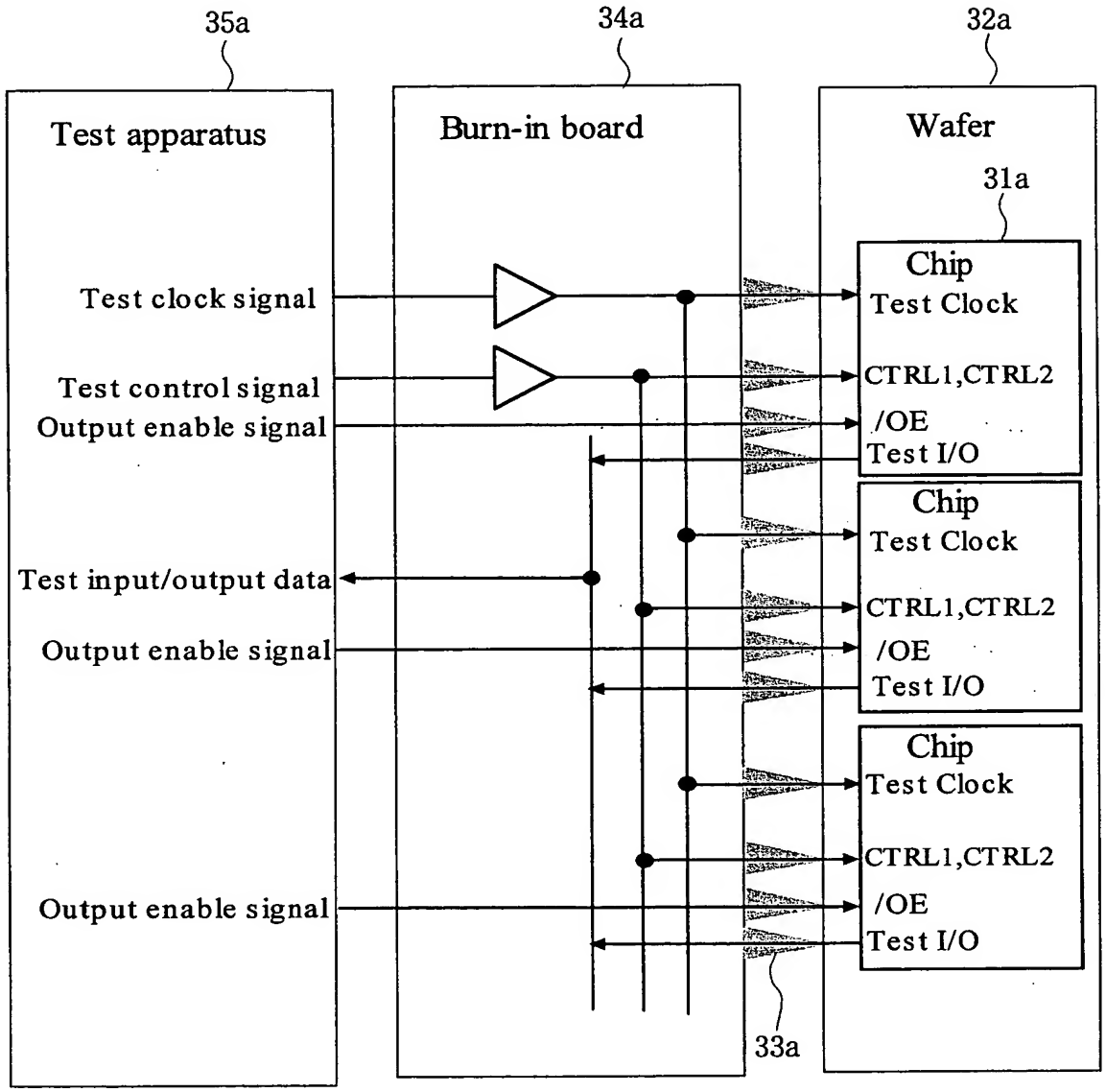

12a
Mode
NAND21
NAND22
A0
DBUF21
A1
DBUF22
A2
DBUF23
AND21
M7
AND22
M6
AND23
M5
AND24
M4
AND25
M3
AND26
M2
AND27
M1
AND28
M0

Fig. 19

A0	A1	A2	Mode	M0	M1	M2	M3	M4	M5	M6	M7
0	0	0	1	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
0	0	0	0	1	1	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0	0	0	0
0	1	0	0	0	0	1	1	0	0	0	0
1	1	0	0	0	0	1	1	0	0	0	0
0	0	1	0	0	0	0	0	1	1	0	0
1	0	1	0	0	0	0	0	1	1	0	0
0	1	1	0	0	0	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0	1	1

Mode=1: Normal decode operation (Always selecting one line)
Mode=0: Multi-choice decode operation (Always selecting two lines)

Fig.20


35a
34a
32a
Test apparatus
Burn-in board
Wafer
31a
Test clock signal
Test control signal
Output enable signal
Test input/output data
Output enable signal
Output enable signal
Chip
Test Clock
CTRL1,CTRL2
/OE
Test I/O
Chip
Test Clock
CTRL1,CTRL2
/OE
Test I/O
Chip
Test Clock
CTRL1,CTRL2
/OE
Test I/O
33a